VITHALBHAI PATEL & RAJRATNA P.T. PATEL SCIENCE COLLEGE
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S.Y. B.Sc. SEM: IV | INTERNAL TEST | DATE: 16th March. 2015
SUB: ELECTRONICS | TIME: 10:30 pm to 12:00 pm
SUB CODE: US04CELE01 | TOTAL MARKS: 25

Q. 1 Choose the correct answer. [03]

(1) The field effect transistor (FET) is a _____ operated devices.
- (A) Voltage
- (B) Current
- (C) Resistance
- (D) None of above

(2) Unit of light intensity is _____ .
- (A) Lumens
- (B) Ampere
- (C) Volts
- (D) None of above

(3) Potential divider Bias circuit in FET is _____ biasing circuit.
- (A) Best
- (B) Not good
- (C) Worst
- (D) None of above

Q.2 Answer the following in short.(Attempt any two, each two marks) [04]

(1) Draw the diagram showing construction and cross section of solar cell.
(2) List different FET parameters and explain any one in brief.
(3) Draw a neat potential divider bias circuit using n-channel FET.

Q.3 Draw a frequency response for transistor amplifier and explain why gain of amplifier falls off at lower frequency end. [06]

OR

Q.3 Explain principle and construction of n-channel JFET and draw the drain characteristics for n-channel JFET and label it. [06]

Q.4 Explain construction and working of n-channel enhancement MOSFET, also draw the diagram showing construction of n-channel enhancement-depletion MOSFET. [06]

OR

Q.4 Give an account of self bias FET circuit. [06]

Q.5 Give an account of photomultiplier tube. [06]

OR

Q. 5 Give an account of LCD (liquid crystal display). [06]

- : All the best: -